(12) UK Patent Application (19) GB (11) 2 382 180 (13) A

(43) Date of A Publication 21.05.2003

(21) Application No 0214098.6

(22) Date of Filing 19.06.2002

(30) Priority Data
(31) 0212260 (32) 28.05.2002 (33) GB

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(51) INT CL[7]
G06F 15/177

(52) UK CL (Edition V)
G4A AFLA
H4L L209 L213

(56) Documents Cited
JP 600230261 A US 6158000 A

(58) Field of Search
UK CL (Edition V) G4A, H4L
INT CL[7] G06F
Other: WPI, EPODOC, PAJ, INSPEC, IBM TDB, IEEE Xplore, Internet

(54) Abstract Title
Processor system wake-up

(57) A method of waking up components in a dual-processor based system. The system includes a first processor system to be activated. Upon activation, components in a second processor based system are required to be likewise activated. The method comprises initiating a wake-up process of a first processor system, waking-up the first processor system components, and generating an interrupt signal. The interrupt signal is passed to the second processor system to initiate a wake-up process of the second processor system components that are required to be woken for the wake-up process of the first processor system. This is performed such that the second processor system components are activated at, or before, a time when the first processor system requires second processor system components to be activated.

A dual processor based system is also described. In this manner, components used in a second processor system, for example a man machine processor system, are awoken in a timely manner when they are needed in the awakening process of the first processor system, for example a GSM processor system to facilitate the periodic scanning of a GSM control channel or timeslots. This prevents delay and reduces power consumption.

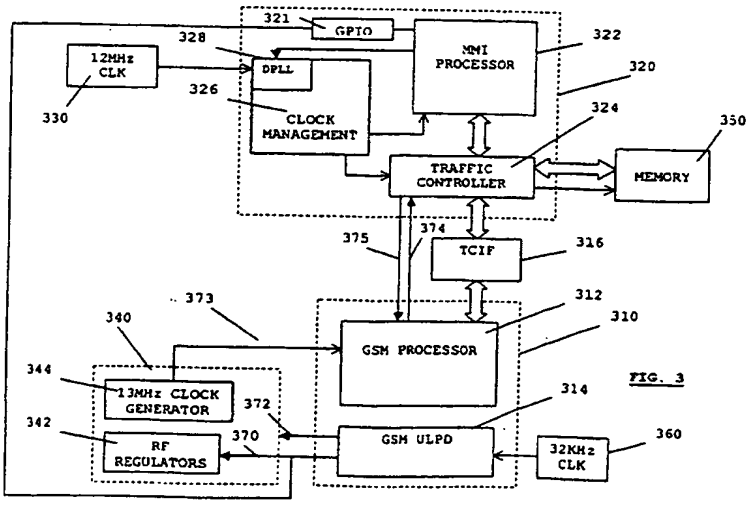

FIG. 3

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

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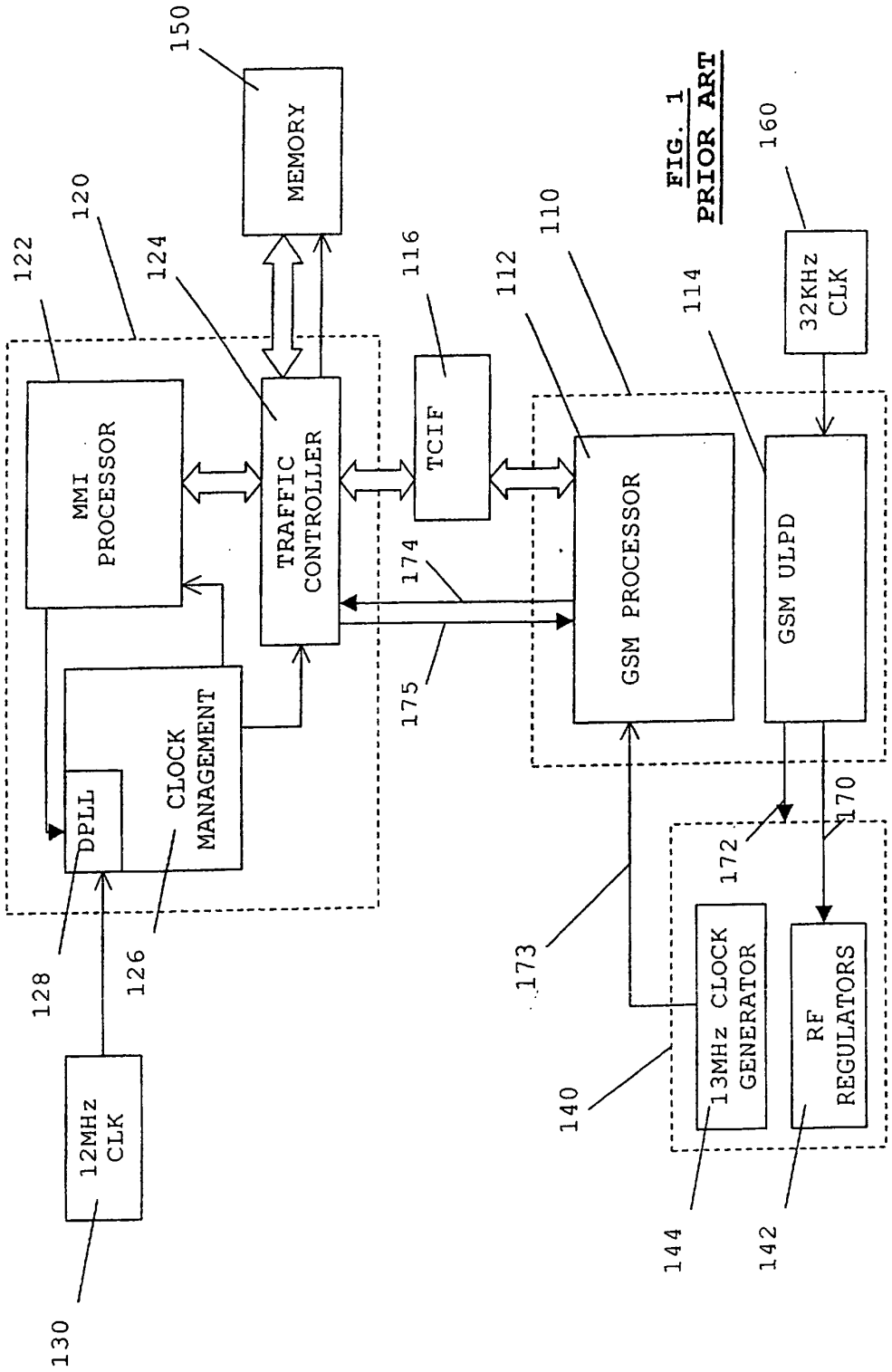

FIG. 1
PRIOR ART

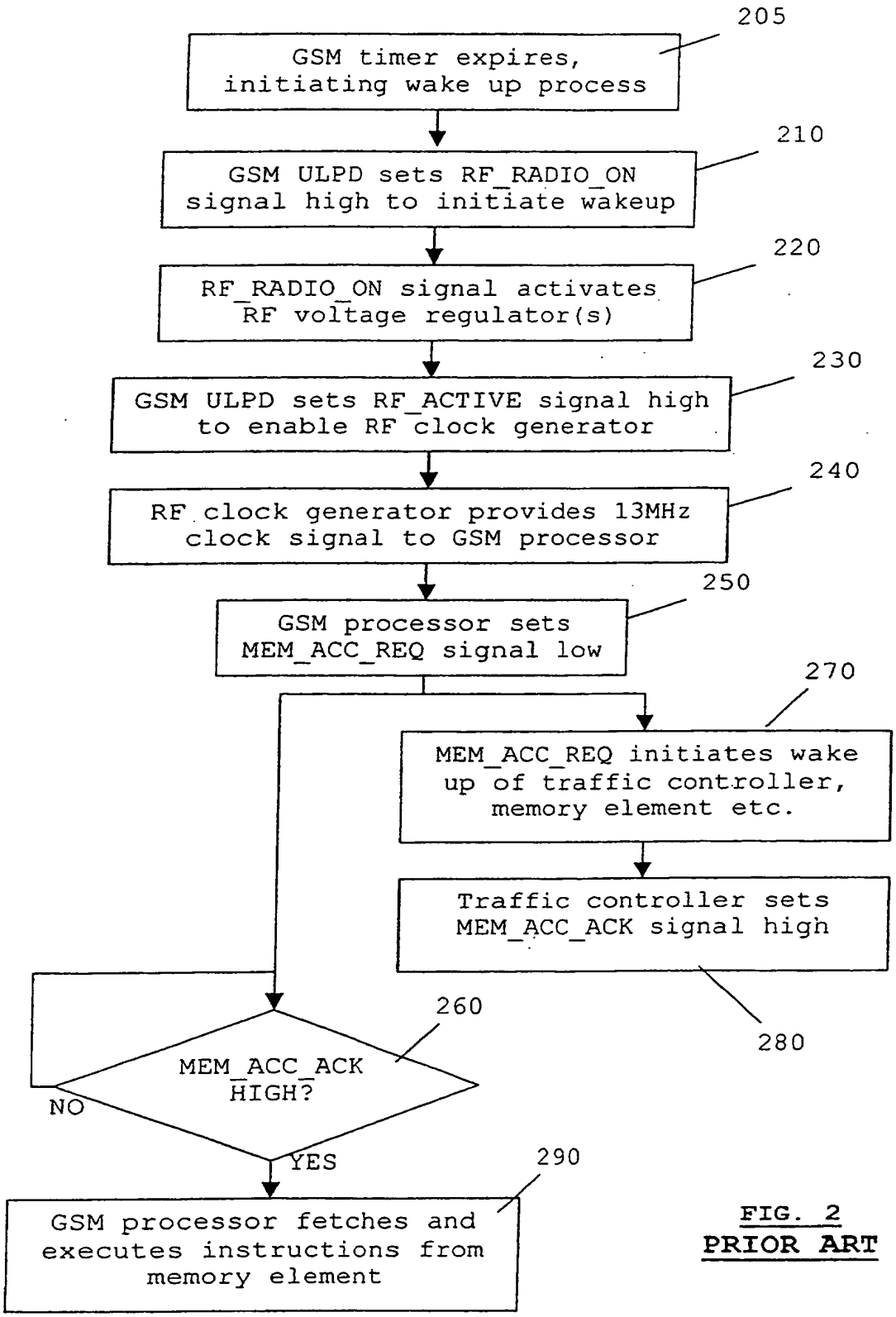

FIG. 2
PRIOR ART

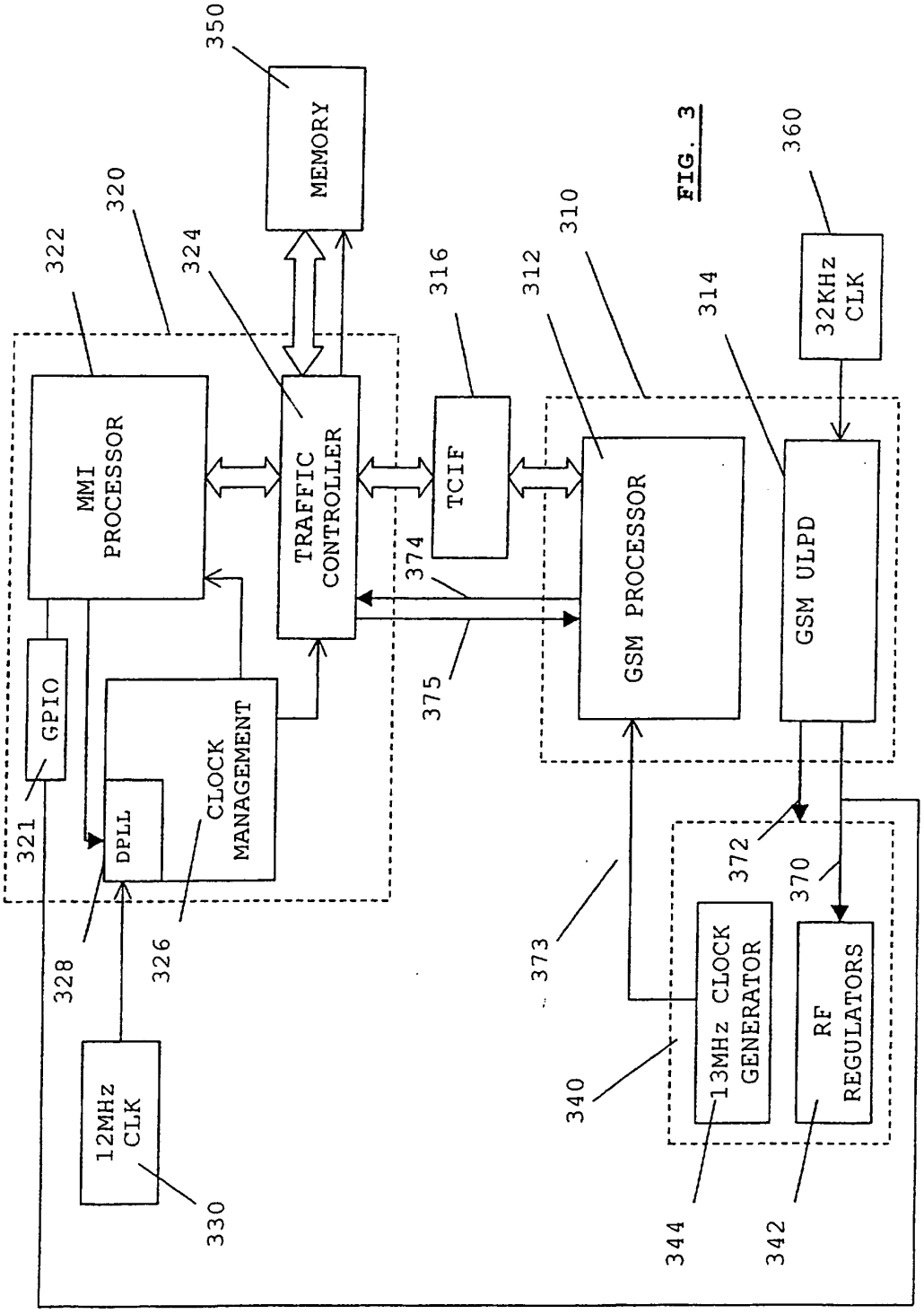

FIG. 3

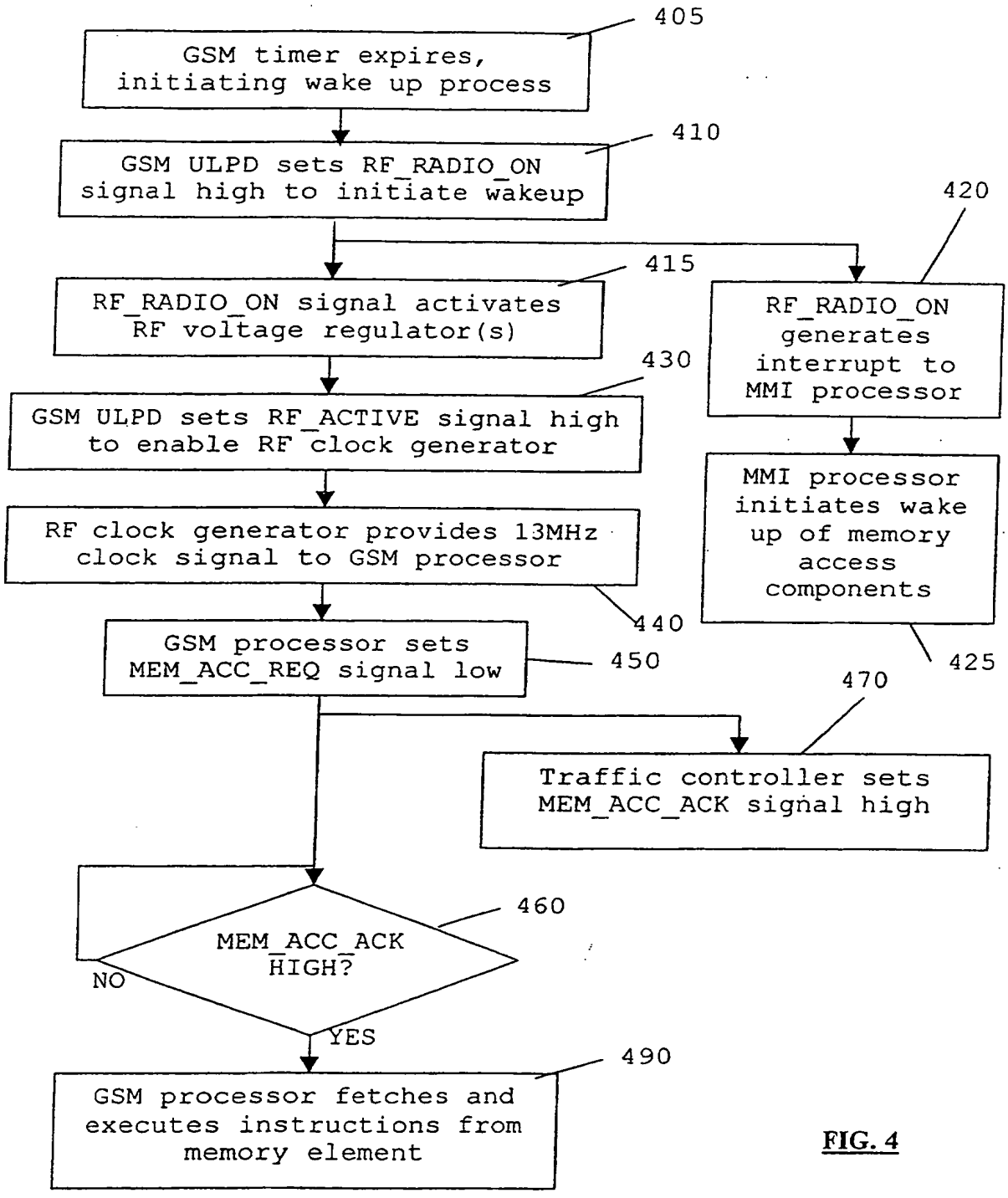

FIG. 4

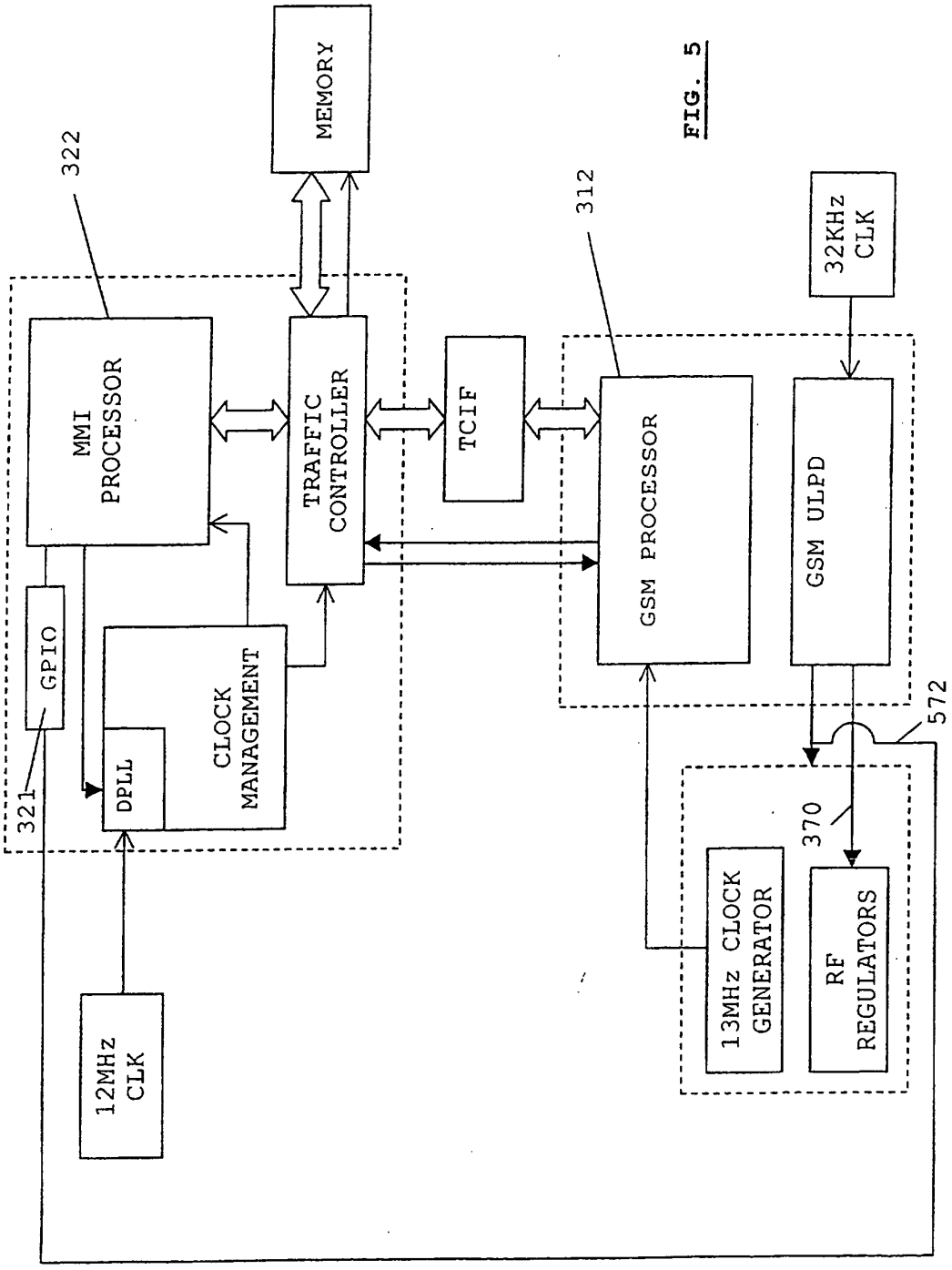

FIG. 5

PROCESSOR SYSTEM WAKE-UP

Field of the Invention

The present invention relates to a process and apparatus for waking up a microprocessor system, in particular a microprocessor system of a radio communications device.

Background of the Invention

It is known for electronic devices such as mobile radio communications devices, which have a limited power supply such as one or more batteries, to make use of various techniques for reducing power consumption. One such technique is to place components, such as microprocessors etc, into sleep modes during times of minimal or no activity, whereby the clock signals provided to the components are reduced in rate or even stopped.

This has the obvious drawback that whilst the components are in sleep mode, their operation is considerably slowed down or even halted. Therefore, it is necessary to 'wake up' the components when they are required to perform an operation.

For devices such as radio communications devices, and in particular, radio communications devices connected to a cellular network such as a Global System for Radio communications (GSM) network or the like, the device spends a large amount of time having no activity from the user. In such circumstances, in order to reduce power

consumption the device will go into sleep mode, as mentioned above. However, in order for the device to operate correctly, it is necessary for it to frequently monitor a control channel of the network cell in which it is camped, as well as perform other periodical activities. This requires at least the RF circuitry and some processing capability to be regularly woken up from sleep mode to monitor the appropriate time slot for the control channel and to then return the device to sleep mode until it is time to monitor the control channel again.

For a communication device connected to a GSM network, it is necessary to monitor the control channel approximately every 0.5 to 2 seconds. In order to keep power consumption to a minimum, only the required components should be brought out of sleep mode, and only for the shortest amount of time necessary. In order to achieve this, the components should be woken up as late as possible, whilst ensuring that they are fully awake in time to monitor the control channel. It is therefore desirable that the process of waking up the components takes the least amount of time possible.

FIG. 1 illustrates a block diagram of a radio communications device indicating the components that are involved in the wake-up process. The radio communications device comprises two processor sub-systems, a GSM sub-system 110 and a man-machine interface (MMI) sub-system 120.

The GSM sub-system 110 is primarily responsible for controlling communication with the network to which the radio communications device is connected, for example handling the GSM protocol stack and signal processing. It also communicates with GSM peripherals (not shown) such as an RF module, baseband/audio CODEC, battery manager, subscriber identification module (SIM) card reader, etc.

The GSM sub-system 110 illustrated comprises a processor 112 and an Ultra-Low-Power Device (ULPD) 114.

The MMI sub-system 120 is primarily responsible for running MMI applications and controlling non-GSM peripherals. Such non-GSM peripherals (not shown) may include a display, keypad, etc. The MMI sub-system may also control components such as USB and/or IrDA interfaces.

The MMI sub-system 120 comprises a processor 122, a traffic controller 124 and a clock management unit 126. The clock management unit 126 comprises a Digital Phased-Locked Loop (DPLL) 128.

Also illustrated is a 12MHz clock generator 130, providing a 12MHz clock signal to the DPLL 128 of the MMI sub-system 120. A 32KHz clock generator 160 provides a 32KHz clock signal to the ULPD 114 of the GSM sub-system 110, part of a radio frequency (RF) module 140, comprising RF voltage regulators 142 and a 13MHz clock generator 144 and a memory element 150. Finally, a traffic controller interface (TCIF) 116 is provided

between the MMI sub-system 120 and the GSM sub-system 110, allowing the GSM processor 112 to access the memory element 150 via the traffic controller 124.

The various components of the overall system, with the exception of the ULPD 114 and clock generators 130 and 160, are capable of being put into sleep mode substantially independently of each other. When a component is put into sleep mode, the clock signal provided to that component is reduced, stopped or blocked.

FIG. 2 illustrates a flow chart of a known process for waking up the GSM sub-system (sub-system 110 of FIG. 1). The GSM ULPD (114 of FIG. 1), which constantly receives a 32KHz clock signal from the clock (160 of FIG. 1), comprises one or more timers to dictate when the GSM sub-system (110 of FIG. 1) is required to wake up.

The process is initiated by the expiration of one such timer in step 205, for example, when it is necessary to monitor the control channel as mentioned above. At the expiration of the timer, the GSM ULPD sets an RF_RADIO_ON signal (170 of FIG. 1) 'high', i.e. a voltage level '1', in step 210.

The RF_RADIO_ON signal activates the RF voltage regulator(s) (142 of FIG. 1), providing a voltage to the RF circuitry (not shown), as illustrated in step 220.

Next, in step 230, the GSM ULPD sets an RF_ACTIVE signal (172 of FIG. 1) 'high'. This enables the RF clock generator (144 of FIG. 1), which generates a 13MHz clock signal (173 of FIG. 1).

The 13MHz clock signal is provided to the GSM processor, thereby waking the GSM processor in step 240. The GSM processor sets a MEM_ACC_REQ signal (174 of FIG. 1) 'low', i.e. a voltage level '0', thereby requesting access to the memory element (150 of FIG. 1) via the traffic controller (124 of FIG. 1), as illustrated in step 250. The GSM processor then waits for an acknowledgement that it has access to the memory element in step 260, indicated by a MEM_ACC_ACK signal (175 of FIG. 1) going 'high'.

When the GSM processor sets the MEM_ACC_REQ signal high, the signal is received, for example, by the traffic controller, which initiates the waking up of the required components, as illustrated in step 270. This provides the GSM processor with access to the memory element, the traffic controller, etc. The DPLL (128 of FIG. 1) and clock management unit (126 of FIG. 1) may also need waking up, in order to provide clock signals to the relevant components.

The amount of time taken for all of the required components to be woken up will depend on each of their states at the time when the request for access to the memory element is made. Once all of the components are awake, the MEM_ACC_ACK signal is set high to indicate

that access to the memory element is available, as illustrated in step 280.

On receipt of the MEM_ACC_ACK signal going high, the GSM processor is able to fetch and execute instructions from the memory element, as illustrated in step 290. The GSM sub-system, and the other required components, is now in an awoken state, and capable of performing the tasks for which it was awoken.

It will be appreciated by those skilled in the art that the GSM processor is capable of executing instructions as soon as it receives the 13MHz clock signal. Indeed this is what the GSM processor does in order to perform the tasks prior to receiving acknowledgement that it has access to the memory element 150. These initial instructions are stored in a local memory (not shown).

However, at least some of the instructions required for carrying out the operation for which the GSM processor 112 was woken up, e.g. monitoring a control channel of the network, are stored in the memory element 150. Therefore, it is necessary for the memory element 150 to also be woken up, as well as the traffic controller 124, clock management unit 126 and TCIF 116.

The inventor of the present invention has recognised that the delay in being able to access the memory element 150 due to the need for it to be woken up is not desirable, since the GSM processor 112 is in a state of waiting until it receives the MEM_ACC_ACK signal 175.

Furthermore, the inventor has recognised that it is preferable that the GSM processor 112 accesses the memory element 150 to begin executing instructions as soon as possible. In this manner, the amount of time required for the sub-system to be out of sleep mode is reduced, and thereby reducing the power consumption of the electronic device.

Furthermore, it is critical that the GSM processor 112 is capable of executing the required instructions for carrying out the operation for which it was woken up at precisely the right time, in order to access the appropriate time slot of, for example, the control channel that it needs to monitor. Therefore, it is necessary for the GSM sub-system 110 to be woken up sufficiently early for a 'worst case scenario' of the amount of time required for all required components to be woken up.

As will be appreciated, this will result in the components being woken up sooner than is necessary on most occasions, and therefore consuming power unnecessarily.

There is therefore a need for an improved process of waking up the GSM sub-system 110, and other required components, that preferably not only reduces the time required for waking up the various components, but in particular reduces the problem of the delay caused in waking up the additional components not forming part of

the GSM sub-system, such as the memory element 150, the traffic controller 124 etc.

In the process described above clock rates used by the MMI sub-system components and the memory element 150 are programmable by the MMI processor 122. The clock rates depend on the settings for the DPLL 128 according to the requirements of the overall system. In the above process, when the DPLL 128 is woken up in order to provide a clock signal for the traffic controller 124, memory element 150 etc, it will use the settings last provided by the MMI processor 122 before going into sleep mode. The inventor of the present invention has recognised that these clock settings may not be optimised for the specific operation required. In this regard, the inventor proposes a mechanism to set the clock rates to reduce the power consumption within the device.

Statement of Invention

According to a first aspect of the present invention there is provided a method of waking up components in a dual-processor based system. A first processor system is to be activated and upon activation requires components in a second processor-based system to be likewise activated. The method includes the steps of initiating a wake-up process of a first processor system, waking-up the first processor system components, and generating an interrupt signal. The interrupt signal is passed to the second processor system to initiate a wake-up process of

second processor system components that are required to be awoken in the wake-up process of the first processor system. Notably, the second processor system components are activated at, or before, a time when the first processor system requires the second processor system components to be activated.

By using the activation/enabling signal provided to, say, the RF circuitry of the first processor system, if it is an air-interface processor system, to initiate the waking up of the second (non air-interface) processor components, the problem of a delay caused in waking up such components is significantly reduced. This is primarily due to the initiation of the waking up of the components being performed earlier on in the overall waking up process, compared to the processor of the first processor sub-system initiating the waking up the components.

Therefore, the overall waking up process is shortened. In this way, the overall waking up process can occur later, reducing the power consumption of the device. Alternatively, by occurring at the same time, the risk that the second processor components are not awake in sufficient time for the task for which they were awoken is reduced.

In a preferred embodiment, the activation or enabling signal may cause a processor of the second processor sub-system to be woken up such that the processor of the second sub-system is able to optimise the components not

associated with the first processor sub-system for use with the processor of the first processor sub-system.

In this way, the clock rates provided to the components not related to the first processor sub-system can be optimised for use with the first processor sub-system, allowing these components, and the first processor sub-system to operate more efficiently.

According to a second aspect of the present invention there is provided a dual-processor based system, for example a cellular communications device comprising an apparatus for waking up a processor sub-system of the cellular communications device.

In a preferred embodiment, the activation or enabling signal may cause a processor of the second processor sub-system to be woken up such that the processor of the second sub-system is able to optimise the components not associated with the first processor sub-system for use with the processor of the first processor sub-system.

Brief Description of the Drawings

FIG. 1 illustrates a block diagram of a known cellular communication device including components involved in a wake up process of the device.

FIG. 2 illustrates a flow chart of a known wake up process of the components of FIG. 1.

Exemplary embodiments of the present invention will now be described, with reference to the accompanying drawings, in which:

FIG. 3 illustrates a block diagram of a cellular communication device including components involved in a wake up process according to a first embodiment of the present invention.

FIG. 4 illustrates a flow chart of a wake up process according to the first embodiment of the present invention.

FIG. 5 illustrates a block diagram of a cellular communication device including components involved in a wake up process according to a second embodiment of the present invention.

Description of Preferred Embodiments

Referring to FIG. 3, a preferred block diagram example illustrates a cellular communication device including components that are involved in a wake up process of a GSM sub-system. The radio communications device comprises two processor sub-systems, a GSM sub-system 310 and an MMI sub-system 320.

The GSM sub-system 310 is primarily responsible for controlling communication with the network to which the radio communications device is connected, for example handling the GSM protocol stack and signal processing. It

also communicates with GSM peripherals (not shown) such as an RF module, baseband/audio CODEC, battery manager, subscriber identification module (SIM) card reader, etc.

The GSM sub-system 310 illustrated comprises a processor 312 and an Ultra-Low-Power Device (ULPD) 314.

The MMI sub-system 320 is primarily responsible for running MMI applications and controlling non-GSM peripherals. Such non-GSM peripherals (not shown) may include a display, keypad, etc. The MMI sub-system may also control components such as USB and/or IrDA interfaces.

The MMI sub-system 320 comprises a processor 322, a traffic controller 324 and a clock management unit 326. The clock management unit 326 comprises a Digital Phased-Locked Loop (DPLL) 328. The MMI sub-system 320 also comprises a general-purpose input/output unit 321.

Also illustrated is a 12MHz clock generator 330, providing a 12MHz clock signal to the DPLL 328 of the MMI sub-system 320. A 32KHz clock generator 360 provides a 32KHz clock signal to the ULPD 314 of the GSM sub-system 310, part of a radio (RF) module 340, comprising RF voltage regulators 342 and a 13MHz clock generator 344 and a memory element 350.

The RF module (not shown) preferably comprises the normal components for radio communications devices, including an antenna, front-end switch, transmit chain, receive chain,

etc. The RF regulators 342, when activated, provide a voltage supply to the other RF components, including the 13MHz clock generator 340. The 13MHz clock generator, when enabled, provides a 13MHz clock signal, which is primarily used as a timing reference signal for the RF circuitry.

Finally, a traffic controller interface (TCIF) 316 is provided between the MMI sub-system 320 and the GSM sub-system 310, allowing the GSM processor 312 to access the memory element 350 via the traffic controller 324.

The various components of the overall system, with the exception of the ULPD 314 and clock generators 330 and 360, are capable of being put into sleep mode substantially independently of each other. When a component is put into sleep mode, the clock signal provided to that component is stopped or blocked.

The block diagram of FIG. 3 is provided for illustrative purposes only, and provides an example of an implementation for the present invention. The present invention is not limited to the specific features thereof. In particular, the present invention is not limited to radio communications devices adapted for use with GSM networks, but rather may be implemented with radio communications devices adapted for use with any radio network, for example General Packet Radio Service (GPRS) or Universal Mobile Telecommunications System (UMTS) networks.

It will be appreciated by those skilled in the art that the various sub-systems illustrated, i.e. the GSM sub-system 310 and the MMI sub-system 320, comprise further components and elements (not shown) in order for them to operate as intended. For example, the GSM sub-system 310 may further comprise an audio digital signal processor (DSP), battery manager, SIM card reader, etc. The MMI sub-system 320 may further include such components as a direct memory access (DMA) controller, display driver, etc. Such further components have been omitted for the sake of clarity, and their omission does not reduce the scope of the present invention.

Furthermore, the present invention is not limited to the various components illustrated and described, and may equally be applied to alternative multi-processor architectures or radio communications devices susceptible to the same problems and disadvantages to which the present invention applies.

According to a first aspect of the present invention there is provided an apparatus for waking up a processor sub-system of a radio communications device, for example the GSM sub-system 310 of the present invention.

The apparatus comprises a timer device, which for the illustrated embodiment is in the form of the GSM ULPD 314, for providing an activation signal or an enabling signal to radio (RF) circuitry of the communications device. The activation signal (RF_RADIO_ON) 370 provided

by the GSM ULPD 314 is received by the RF regulators 342 in order to provide a voltage supply to the RF circuitry.

The activation signal is provided to the RF regulators 342 prior to a processor of the first processor sub-system, i.e. the GSM processor 312, being awoken.

The activation signal is also provided to a second processor sub-system, which for the illustrated embodiment is the MMI sub-system 320. In this regard, the activation signal initiates the waking up of components not associated with the GSM sub-system 310 that are required for a task for which the GSM sub-system is to be woken up for. For example, those components required for the access of memory by a processor of the first processor system. For the illustrated embodiment, such components may include the clock management unit 326, traffic controller 324, memory element 350 etc.

In the illustrated embodiment, the GSM ULPD 314 provides a second signal to the RF circuitry. This second signal (RF_ACTIVE) 372 enables the 13MHz clock generator 344, which 'starts up' the RF circuitry (not shown). The 13MHz clock generator 344 also provides a clock signal 373 to the GSM processor 312, waking up the GSM processor 312.

By using the activation/enabling signal provided to the RF circuitry to initiate the waking up of the components not associated with the first processor sub-system, the problem of a delay caused in waking up such components is significantly reduced. This is primarily due to the

initiation of the waking up of the components being performed at an earlier time in the overall waking up process, compared to the processor of the first processor sub-system initiating the waking up the components.

Therefore, the overall waking up process is shortened. In this way, the overall waking up process can occur later, reducing the power consumption of the device. Alternatively, if the waking process commences at the same time, it reduces the risk that the components not associated with the first processor sub-system are not awake in sufficient time for the purpose of waking up to be performed.

The activation or enabling signal preferably causes a processor of the second processor sub-system, which for the present invention is the MMI processor 312, to be woken up. In this way the MMI processor 312 is able to optimise the required components, not associated with the GSM sub-system 310, for use with the GSM processor 312.

In this way, the clock rates provided to the components not related to the first processor sub-system can be optimised for use with the first processor sub-system, allowing these components, and the first processor sub-system to operate more efficiently.

For the illustrated embodiment, the activation signal RF_RADIO_ON 370 is provided to a general purpose input/output (GPIO) port of the MMI sub-system 320. This

provides an interrupt to the MMI processor 322 when the activation signal RF_RADIO_ON 370 is set.

According to a further aspect of the present invention there is provided a method of waking up a first processor sub-system of a radio communications device.

The method comprises the first step of providing either an activation signal or an enabling signal to radio frequency (RF) circuitry of the radio communications device prior to or substantially at the same time as waking up a processor of the first processor sub-system.

The method comprises the further step of also providing the activation or enabling signal to a second processor sub-system in order to initiate the waking up of components not associated with the first processor sub-system that are required for a task for which the first processor sub-system is to be woken up for.

In a preferred embodiment, the activation or enabling signal may cause a processor of the second processor sub-system to be woken up such that the processor of the second sub-system is able to optimise the components not associated with the first processor sub-system for use with the processor of the first processor sub-system.

FIG. 4 illustrates a flow chart of a preferred implementation of the method of the present invention, using the apparatus illustrated in FIG. 3.

The GSM ULPD (314 of FIG. 3), which constantly receives a 32KHz clock signal from the clock (360 of FIG. 3), comprises timers for when the GSM sub-system (310 of FIG. 3) is required to wake up.

The method is initiated by the expiration of one such timer in step 405, for example, when it is necessary to monitor the control channel as mentioned above. At the expiration of the timer, the GSM ULPD sets an RF_RADIO_ON signal (370 of FIG. 3) 'high', i.e. a voltage level '1', in step 410.

The RF_RADIO_ON signal activates the RF voltage regulator(s) (342 of FIG. 3), as illustrated in step 415.

As will be appreciated by those skilled in the art, the RF circuitry (not shown) is enabled prior to the GSM sub-system, and other components, due to the time required for the RF circuitry to stabilise. Typically, the RF circuitry comprises a transmit chain, a receive chain, a controller for controlling the transmit and receive chains, an antenna and a front-end switch for coupling the transmit and receive chains to the antenna. RF circuitry is well known in the art, and so will not be described further.

The RF_RADIO_ON signal is also provided to the GPIO unit (321 of FIG. 3) of the MMI sub-system (320 of FIG. 3), generating an interrupt to the MMI processor (322 of FIG. 3), as illustrated in step 420. If necessary, the interrupt signal wakes the MMI processor. In step 425,

the MMI processor recognises the interrupt as originating from the GSM sub-system and initiates the wake up process for the components required by the GSM processor (312 of FIG. 3) to perform the task for which it was woken up. Such components may be those required to access the memory element (350 of FIG. 3), the traffic controller (324 of FIG. 3), etc. The DPLL (328 of FIG. 3) and clock management unit (326 of FIG. 3) may also need waking up, in order to provide clock signals to the relevant components. This may be achieved by sending an appropriate signal to the traffic controller.

In such a case, although not illustrated, when the traffic controller is in sleep mode, preferably an automatic request (e.g. generated by hardware logic) is sent to a clock management unit to generate a clock signal for the traffic controller. The request causes an interrupt, which if needed wakes the clock management unit. The resulting clock signal wakes the traffic controller, allowing it to initiate the wake up of the required components.

The amount of time taken for all of the required components to be woken up will depend on each of their states at the time when the request for access to the memory element is made.

Thus, wake up of the components required for memory access is initialised prior to waking up of the GSM processor.

Advantageously, the MMI sub-system components are then awake and in a functional operational state when required by the GSM sub-system.

Once the MMI processor has initiated the wake up of the components required for accessing the memory element, it preferably reverts to a sleep mode, assuming that no further activity is required of it.

Meanwhile, in step 430, the GSM ULPD sets an RF_ACTIVE signal (372 of FIG. 3) 'high'. This enables the RF clock generator (344 of FIG. 3), which generates a 13MHz clock signal (373 of FIG. 3).

The 13MHz clock signal is provided to the GSM processor, thereby waking the GSM processor in step 440. The GSM processor sets a MEM_ACC_REQ signal (374 of FIG. 3) 'low', i.e. a voltage level '0', thereby requesting access to the memory element via the traffic controller, as illustrated in step 450, and then waits for an acknowledgement that it has access to the memory element in step 460, indicated by a MEM_ACC_ACK signal (375 of FIG. 3) going 'high'.

When the GSM processor sets the MEM_ACC_REQ signal high, the traffic controller receives the signal, for example. Since the MMI processor has already initiated the wake up of the required components, and preferably by this point the components are already awake, the traffic controller sets the MEM_ACC_ACK signal high to indicate that access

to the memory element is available, as illustrated in step 470.

If, however, the components are still in the processes of being woken up, the traffic controller preferably waits until all the components are awake before setting the MEM_ACC_REQ signal high.

On receipt of the MEM_ACC_ACK signal going high, the GSM processor is able to fetch and execute instructions from the memory element, as illustrated in step 490. The GSM sub-system, and the other required components, is now in an awoken state, and capable of performing the tasks for which they it was awoken.

It will be appreciated that, although not described or illustrated, other operations may also be required in the wake up process. For example, the GSM processor 312 may require a faster clock signal, for example, a 32MHz clock signal, which is provided from a further clock generator or DPLL (not shown). Such further operations have been omitted for clarity, and do not affect the scope of the present invention.

It will be appreciated by those skilled in the art that the GSM processor 312 is capable of executing instructions as soon as it receives the 13MHz clock signal 373. Indeed the GSM processor 312 preferably does this in order to perform the tasks prior to receiving acknowledgement that it has access to the memory element

350. These initial instructions are stored in a local memory (not shown).

However, at least some of the instructions required for carrying out the operation, for which the GSM processor 312 was woken up, e.g. monitoring a control channel of the network, are stored in the memory element 350. Therefore, it is necessary for the memory element 350 to also be woken up, as well as the traffic controller 324, clock management unit 326, TCIF 316, and any other components necessary for the GSM processor 312 to access the memory element 350.

The delay in being able to access the memory element in the prior art process described above, caused by having to wait for the memory element, traffic controller, etc. to be woken up, is substantially overcome, or at least significantly reduced, since the MMI processor 322 initiates the waking up of these components at an earlier stage. Hence, the components will be awake sooner, preferably by the time the GSM processor 312 requests access to the memory element 350.

Thus, the GSM processor 312 is preferably not in a state of waiting until it receives the MEM_ACC_ACK signal 175 for any significant amount of time. In this regard, the GSM processor 312 is able to begin executing instructions as soon as possible, thereby reducing the amount of time required for the sub-system to be out of sleep mode. This, in turn, reduces the power consumption of the electronic device.

Furthermore, the GSM processor 312 is able to execute the required instructions for which it was woken up at precisely the right time. Hence, the GSM processor 312 is able to access the appropriate time slot of, for example, the control channel that it needs to monitor. This significant improvement is due to the reduction in the need to wait for the awakening of the memory element 350, traffic controller 324 etc.

Thus, the present invention provides an improved process of waking up a processor sub-system, and any other required components, which reduces the aforementioned delay problem. In this manner, any delay caused in waking up any additional components not forming part of that processor's sub-system is mitigated, allowing the processor's sub-system and components to be woken up at a later stage. Advantageously, this in turn reduces the power consumption of the device.

Although in the illustrated embodiment MEM_ACC_ACK and MEM_ACC_REQ signals have been used to determine when access to the memory element is available to the GSM (or other) processor, the present invention is not limited to such signals, and any other form of notification to the GSM (or other) processor may alternatively be used.

As previously mentioned, the inventor of the present invention has recognised a further mechanism to improve a processor system wake-up operation. In this regard, the clock rates used by the MMI sub-system components and the

memory element 150 depend on the settings for the DPLL 128 and clock management unit 126 according to the requirements of the overall system. In the prior art process of FIG. 1, when the DPLL 128 is woken up in order to provide a clock signal for the traffic controller 124, memory element 150 etc, it will use the settings last provided by the MMI processor 122 before going into sleep mode. Therefore, the clock settings may not be optimised for the specific operation required.

For example, the GSM processor 110 operates at 32MHz. It therefore receives a 32MHz clock signal from a clock generator (not shown) once it has been woken up. The MMI processor 120 operates at 120MHz. Therefore, when only the GSM processor 110 is required, for example when the communications device is in an idle state and the GSM processor 110 is accessing the network or monitoring the control channel of the serving cell, the clock rates for the memory element 150, traffic controller 124 etc, may be kept reasonably low. Thus, the inventor has appreciated that these clock rates do not need to be as high for optimal operation with the GSM processor 110 as for when the MMI processor 120 is fully operational. If the clock rates provided to the memory element 150, traffic controller 124 etc. are optimised for operation with the MMI processor 120 when woken up, the devices will be consuming more power than is necessary.

In accordance with an enhanced embodiment of the present invention, the MMI processor 322, on receiving the interrupt from the RF_RADIO_ON signal 370, preferably

also configures the DPLL 328 and clock management unit 326 to provide clock signals optimised for the GSM sub-system 310. In this way, the power consumption of the relevant components is also minimised.

In summary, the process of the present invention allows the GSM sub-system 310 to be ready to monitor the control channel in a shorter amount of time. Thus, the GSM sub-system 310 can be woken up at a later than usual time. This not only makes the GSM sub-system 310 more reliable, since the risk of not being ready to execute the required instructions is reduced, but also reduces the power consumption of the device.

In summary, this is achieved by utilising an initial activation signal provided to the RF circuitry to also initialise the wake up of components required for accessing e.g. a memory element, which does not form a part of the GSM sub-system 310. In this way, the waking up of these required components, such as the memory element 350, traffic controller 324 etc, is initiated at least at the same time as the waking up of the GSM sub-system 310, and preferably prior to the waking up of the GSM sub-system 310. This allows the memory element to be accessible to the GSM processor 312 earlier, and preferably as soon as required by the GSM processor 312.

Another advantage of the preferred embodiment of the present invention is that the MMI processor 322 is also able to optimise the clock rates provided to the various

components for operation with the GSM processor 312. In this way, the power consumption is further optimised.

FIG. 5 illustrates an alternative embodiment of the present invention. This embodiment differs from the embodiment illustrated in FIG. 3 (and flowchart of FIG. 4) in that the RF_ACTIVE signal 572 is provided to the GPIO unit 321, instead of the RF_RADIO_ON signal 370. In this way the MMI processor 322 and the GSM processor 312 will be woken up at substantially the same time.

In both embodiments illustrated and described, the use of signals provided to the RF circuitry, namely the RF_RADIO_ON and the RF_ACTIVE signals, to wake up the MMI processor reduces the amount of time in which the GSM processor is able to access the memory element.

Thus, the GSM sub-system is able to remain in a sleep mode for longer, reducing the power consumption.

By using the activation/enabling signal provided to the RF circuitry to initiate the waking up of the components not associated with the first processor sub-system, the problem of a delay caused in waking up such components is significantly reduced. This is primarily due to the initiation of the waking up of the components being performed earlier on in the overall waking up process, compared to the processor of the first processor sub-system initiating the waking up the components.

Therefore, the overall waking up process is shortened. In this way, the overall waking up process can occur later, reducing the power consumption of the device. Alternatively, by occurring at the same time the risk that the components not associated with the first processor sub-system are not awake in sufficient time for the purpose of waking up to be performed is reduced.

In a preferred embodiment, the activation or enabling signal may cause a processor of the second processor sub-system to be woken up such that the processor of the second sub-system is able to optimise the components not associated with the first processor sub-system for use with the processor of the first processor sub-system.

In this way, the clock rates provided to the components not related to the first processor sub-system can be optimised for use with the first processor sub-system, allowing these components, and the first processor sub-system to operate more efficiently.

All other features and implementations herein described and/or illustrated in the drawings are considered solely as preferred additions and/or alternatives, and are not limiting on the scope of the present invention.

Whilst the specific and preferred implementations of the embodiments of the present invention are described above, it is clear that one skilled in the art could readily apply variations and modifications of such inventive concepts.

Claims

1. A method of waking up components in a dual-processor based system, wherein a first processor system is to be activated and upon activation requires components in a second processor based system to be likewise activated, the method comprising the steps of:

initiating a wake-up process of a first processor system;

waking-up said first processor system components;

generating an interrupt signal;

passing said interrupt signal to said second processor system to initiate a wake-up process of said second processor system components that are required to be woken upon the wake-up process of said first processor system, such that said second processor system components are activated at, or before, a time when said first processor system requires second processor system components to be activated.

2. The method of waking up components in a dual-processor based system according to Claim 1, wherein said dual-processor based system resides in a wireless communication device, having a first air-interface processor system, for example a GSM processor system, and a second non-air interface processor system, for example a man machine interface processor system.

3. The method of waking up components in a dual-processor based system according to Claim 1 or Claim 2, wherein said step of generating an interrupt signal is

generated substantially at the same time or before said first processor system components are activated.

4. The method of waking up components in a dual-processor based system according to Claim 2 or Claim 3, wherein said step of generating an interrupt signal, incorporates the step of re-using a trigger signal that activates radio frequency components of said first air-interface processor system in said first processor system.

5. The method of waking up components in a dual-processor based system according to any preceding Claim, wherein said step of generating an interrupt signal includes the step of:

awakening a second processor in said second processor system; and

controlling a wakening process of said second processor components by said second processor.

6. The method of waking up components in a dual-processor based system according to Claim 5, wherein said step of controlling includes the step of:

adapting one or more clock rates used to operate said second processor system components to substantially comply with clock rates used in said first processor system.

7. The method of waking up components in a dual-processor based system according to any preceding Claim, the method further characterised by the step of:

waking-up components requiring memory access prior to waking up components that do not require memory access.

8. A dual-processor based system, comprising:

a first processor system to be activated,

a second processor system, operably coupled to said first processor system, comprising second processor system components required in said activation of said first processor system; and

a timer function, operably coupled to said first processor system to generate an activation or enabling signal to activate one or more components in said first processor system,

wherein said activation or enabling signal is applied to one or more second processor system components to initiate a wake-up process of said second processor system components, such that said second processor system components are activated at, or before, a time when said first processor system requires said second processor system components to be activated.

9. The dual-processor based system according to Claim 8, wherein said dual-processor based system resides in a wireless communication device, having a first air-interface processor system, for example a GSM processor system, and a second non-air interface processor system, for example a man machine interface processor system.

10. The dual-processor based system according to Claim 8 or Claim 9, wherein said timer function is controlled

by a first processor in said first processor system and applies said activation or enabling signal to said second processor system components substantially at the same time or before said first processor system components are activated.

11. The dual-processor based system according to Claim 9 or Claim 10, wherein said activation or enabling signal is used in said first processor system to activate radio frequency components of a first air-interface processor system, for example a GSM processor system.

12. The dual-processor based system according to any of preceding Claims 8 to 11, wherein said timer function adapts one or more clock rates used to operate said second processor system components such that said clock rates substantially comply with clock rates used in said first processor system.

13. The dual-processor based system according to any of preceding Claims 8 to 12, the dual-processor based system further characterised by:

a memory element, operably coupled to said first processor system and said second processor system such that said timer first activates components that require memory access prior to waking up components that do not require memory access.

14. A method of waking up components in a dual-processor based system substantially as hereinbefore

described with reference to, and/or as illustrated by, FIG 3 of the accompanying drawings.

15. A dual-processor based system substantially as hereinbefore described with reference to, and/or as illustrated by, FIG 4 or FIG. 5 of the accompanying drawings.

Application No:	GB 0214098.6	**Examiner:**	Michael Powell Waters
Claims searched:	1 to 15	**Date of search:**	3 April 2003

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
X	1 and 8	US 6158000	(COLLINS) for example see column 7 lines 1 to 19
X	1 and 8	JP 600230261 A	(SHIBAURA) see PAJ abstract

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G4A, H4L

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The following online and other databases have been used in the preparation of this search report :

WPI, EPODOC, PAJ, INSPEC, IBM TDB, IEEE Xplore, Internet